

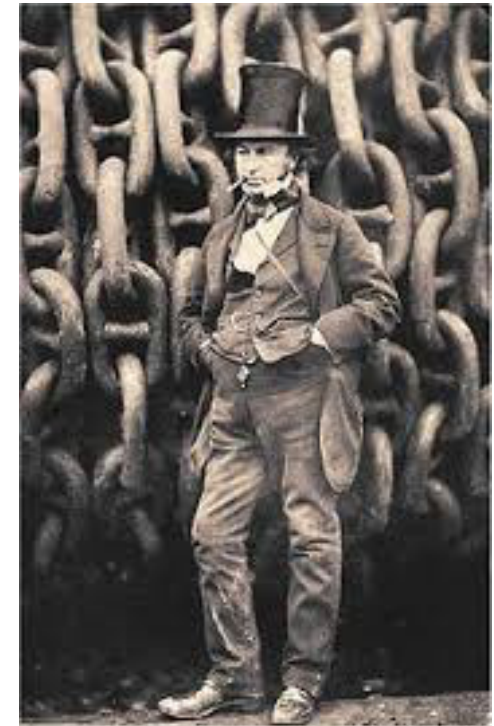
# *First public disclosure of Isambard performance results*

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## Why explore Arm-based supercomputers?

- The architecture development is driven by the *fast-growing mobile space*
- Multiple vendors of Arm-CPU:
  - Greater **competition**
  - More **choice**
  - Rapid **innovations**, e.g. in vector instruction set
- **MONT-BLANC** proved the approach is feasible

**'Isambard', a new Tier 2 HPC service from GW4.  
Named in honour of Isambard Kingdom Brunel**



I.K.Brunel 1804-1859

**Tier 0: international**

DoE



**The tiered model of  
HPC provision**

**Tier 1: national**



**Tier 2: regional**

TIER 2 HPC CENTRES

Edinburgh

Cambridge

University College,  
London

Loughborough

Bristol

Oxford

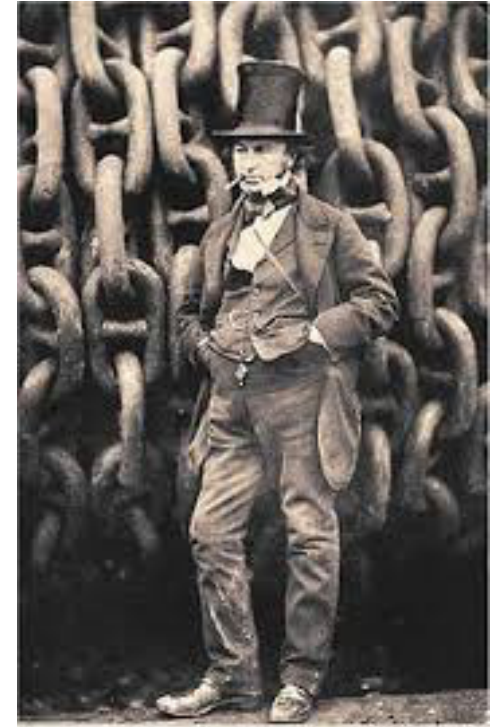
**Tier 3**



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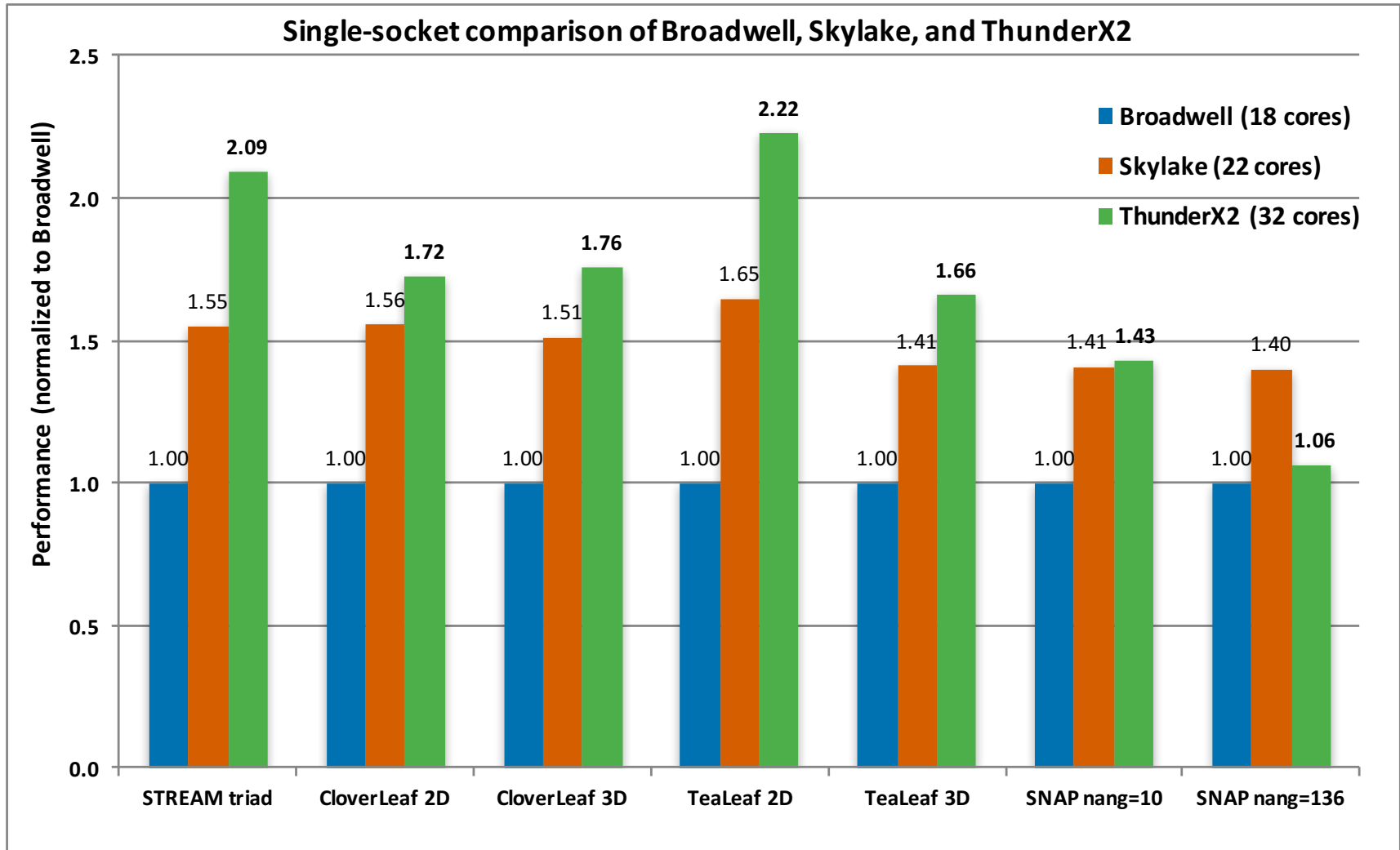
## Isambard system specification (red = new info):

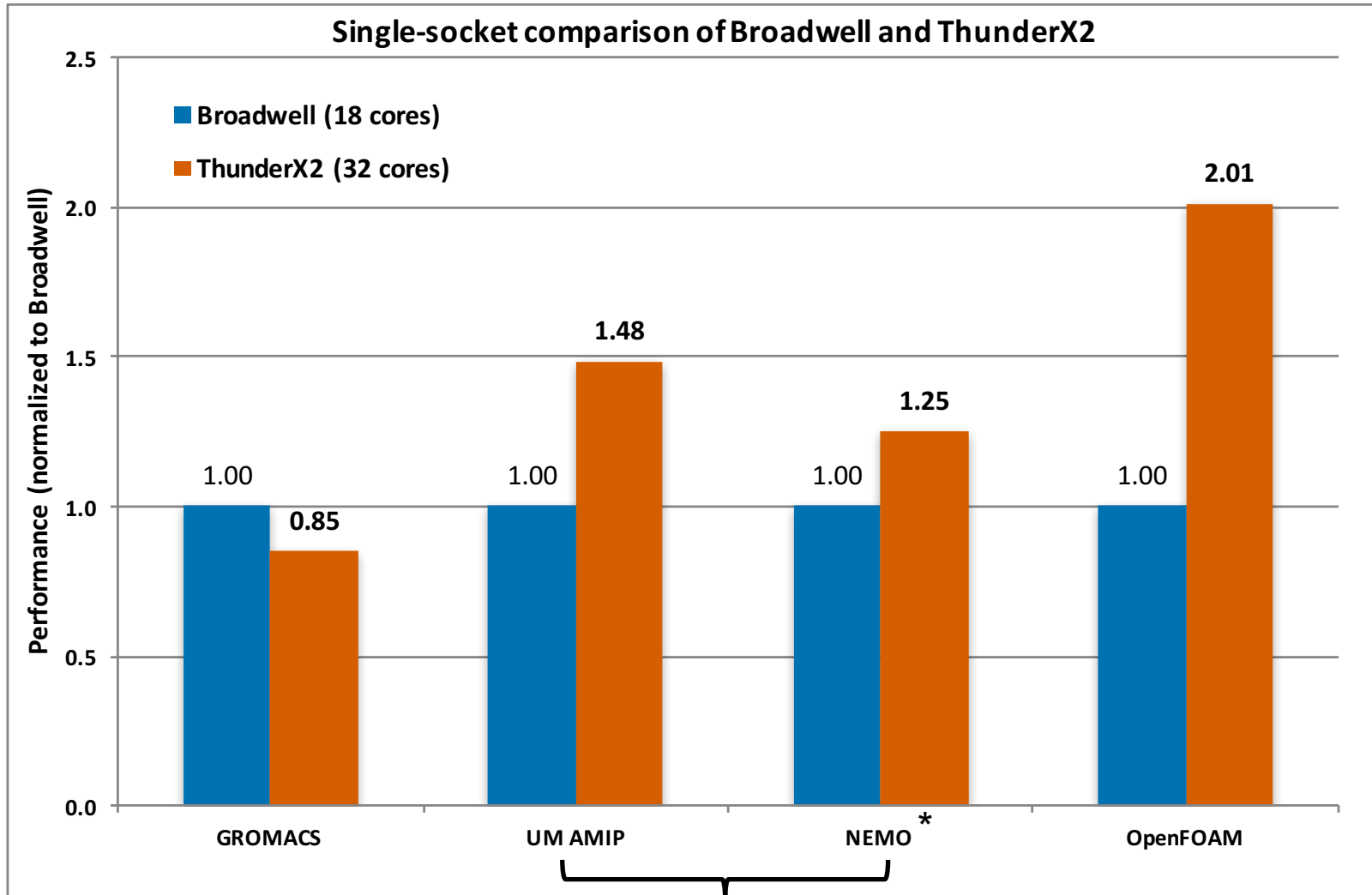
- Cray “**Scout**” system – **XC50 series**
  - **Aries interconnect**
- **10,000+** Armv8 cores
  - **Cavium ThunderX2 processors**
  - **2x 32core @ >2GHz per node**
- Cray software tools
- Technology comparison:
  - x86, Xeon Phi, Pascal GPUs
- Phase 1 installed March 2017
- The Arm part arrives early 2018



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- The Isambard project's focus will be on the top 10 most heavily used codes on Archer in 2017:
    - VASP, CASTEP, GROMACS, CP2K, UM, HYDRA, NAMD, Oasis, SBLI, NEMO
    - Note: 8 of these 10 codes are written in **FORTRAN**
  - Additional important codes for project partners:
    - OpenFOAM, OpenIFS, WRF, CASINO, LAMMPS, ...
  - We want to collaborate wherever possible!
    - Accelerate the adoption of Arm in HPC







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## Details for benchmarks comparisons:

- ThunderX2 early access systems
  - 32c, 2.5GHz, 2667MHz DDR4, Ubuntu 16.04
  - 28c, 2.0GHz, 2400MHz DDR4, SLES 12 SP3
  - All alpha release (pre-production) hardware
- Broadwell system
  - 18c, 2.1GHz, 2400MHz DDR4, Xeon E5-2695 v4
- Skylake system
  - 22c, 2.1GHz, 2667MHz DDR4, Xeon Gold 6152

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### Software used for ThunderX2:

- UM, NEMO and TeaLeaf: Cray CCE 8.6.4
  - UM and NEMO results produced by the UK's Met Office
- GROMACS, OpenFOAM and STREAM: GCC 7.1
- CloverLeaf: 2D armflang 18.0, 3D armflang 1.4
- SNAP: nang=10 armflang 1.4, nang=136 CCE 8.6.3

### Software used for Broadwell:

- UM and NEMO: Cray CCE 8.5.8, produced by the Met Office
- GROMACS: GCC 7.1
- Intel 2017 compiler for everything else

### Software used for Skylake:

- Intel 2018 compiler

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## Benchmark test case parameters:

- **UM AMIP** (v10.8): 6day
- **NEMO**: GYRE\_PISCES, idealised calculation, 720 timesteps
- **GROMACS**: rnase\_cubic
- **OpenFOAM**: motorBike
- **STREAM**: test size of  $2^{25}$  double precision elements per array with 100 iterations
- **CloverLeaf**: 2D bm\_16, 3D bm1s\_short
- **TeaLeaf**: 2D bm\_5, 3D bm\_3 0.04
- **SNAP**: 1024x16x(NC/2), ng=32

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Other applications being ported to Isambard include:

VASP, CASTEP, CP2K, HYDRA, NAMD, Oasis, SBLI, OpenIFS, WRF,  
CASINO, LAMMPS...

Early results suggest that for compute-bound applications such as GROMACS, CP2K and VASP, performance between the different processors is closer than for memory bandwidth bound codes. This is because, while the codes benefit from the wider vector units of the x86 processors, ThunderX2 compensates with higher core counts and clock speeds

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## For more information:

- <http://gw4.ac.uk/isambard/>
- <http://investors.cray.com/phoenix.zhtml?c=98390&p=irol-newsArticle&ID=2316352>
- <https://github.com/UoB-HPC/GW4-Isambard>
- Twitter: @simonmcs
- Email: [simonm@cs.bris.ac.uk](mailto:simonm@cs.bris.ac.uk)